ABSTRACT OF THE DISCLOSURE

The interconnect pin count between field programmable gate arrays (FPGAs) used in prototyping an application specific integrated circuit (ASIC) is reduced without compromising the prototyping by using serial links between the FPGAs. A block A of the ASIC is programmed in a first FPGA. A block B of the ASIC is programmed in a second FPGA. Blocks A and B are identical between ASIC and FPGA implementations. Block A communicates with block B via two interconnected wrappers, which are, in this example, serial COM wrappers connected by a serial link.